Amendments to the Specification:

Please replace the paragraph beginning at page 4, line 20, with the following rewritten paragraph:

Referring now to FIG. 1, FIG. 1 is a block diagram of an example of a system-on-chip integrated circuit 10 that includes a DMA communication system. The DMA communication system includes a DMA module 20 which is coupled to a plurality of hardware resources including one or more universal asynchronous receiver-transmitters (UARTs) 23, one or more serial interfaces 25 for interfacing to external devices (such as digital-to-analog converters (DACs), audio controllers, and so on), and one or more memory controllers 27 and 28. The DMA module is coupled to these devices by way of a data bus 30 and a DMA access request bus 35. In practice, the data bus 30 may include separate high speed bus and low speed busses. The resources 23, 25, ~~and~~ 27, and 28 are connected to the data bus 30, and are accessible by the DMA modules.

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Please replace the paragraph beginning at page 5, line 9, with the following rewritten paragraph:

In addition to the resources 23, 25, ~~and~~ 27, and 28, there are a plurality of additional devices that are part of the integrated circuit 10 but that are not a source or destination resources for DMA transfers on the data bus 30. These devices include a microprocessor 40, interrupt controller/timers 42, a keypad interface 44, one or more I/O ports 46, a touch screen interface circuit 48, one or more universal serial bus (USB) host interfaces 50 for connection to USB devices such as a keyboard, mouse, printer, and so on, an Ethernet port 52, a display interface 54 (for example, a raster engine), and boot ROM 56 for storing program code executed during a boot-up sequence.

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Please replace the paragraph beginning at page 5, line 18, with the following rewritten paragraph:

Likewise, in addition to the hardware resources 23, 25, 27, and 28, there may be a plurality of additional hardware resources (not shown in FIG. 1) which are either a source or destination resources during a DMA transfer on the data bus 30 but which are not part of the

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system-on-chip integrated circuit 10. These resources are referred to as external hardware resources. A computer system that utilizes the system-on-chip integrated circuit 10 is unlikely to utilize all of the internal hardware resources and is likely to use some external resources. For example, assuming the system-on-chip integrated circuit 10 includes multiple UARTs and serial ports, only a portion of the UARTs and serial ports may be utilized, depending on how the system-on-chip integrated circuit 10 is configured.

Please replace the paragraph beginning at page 5, line 28, with the following rewritten paragraph:

Referring now to FIG. 2, FIG. 2 is a block diagram showing the DMA module 20 of FIG. 1 in greater detail. In FIG. 2, the hardware resources have been renumbered to facilitate explanation of the DMA module 20, as will become clear below. The hardware resources (including the hardware resources 23, 25, ~~and~~ 27, and 28 as well as any external hardware resources) are designated with the reference numerals 60-0 through ~~60-M~~ 60-N. Herein, the reference numerals 60-0 through ~~60-M~~ 60-N are used to refer to the hardware resources individually, and the reference numeral 60 is used to refer to the hardware resources collectively. (This scheme will be used in connection with other structures/reference numerals as well.) The hardware resources 60 may comprise a combination of some of the hardware resources 23, 25, ~~and~~ 27, and 28 and a plurality of external hardware resources, although the particular combination is likely to vary depending on the application. The particular composition of the hardware resources is not important.

Please replace the paragraph beginning at page 6, line 22, with the following rewritten paragraph:

The DMA module 20 includes a plurality of DMA controllers 70. (Again, to refer to the DMA controllers individually, the reference numerals 70-0 to ~~70-M~~ 70-N are used.) In general, any resource 60 may be associated with any DMA controller 70. The DMA controllers 70 each include a register 72 that associates the particular controller 70 with a particular one of the hardware resources 60. For example, if there are sixteen total available hardware resources (including both active and inactive hardware resources), then the register

a5 is a four bit register allowing for sixteen different values. Any hardware resource 60 that is not associated with one of the controllers 70 is thereby rendered inactive.